1 MHz – 10 GHz, 50 dB Log Detector/Controller

Preliminary Technical Data

AD8317

FEATURES

Wide bandwidth: 1 MHz to 10 GHz
High accuracy: ±1.0 dB over temperature
>50 dB Dynamic Range up to 5.8 GHz
Stability over temperature ±0.5 dB
Low noise measurement/controller output VOUT
Pulse response time 8/10 nS (fall/rise)
Small footprint 2mm x 3mm CSP package
Supply operation: 3.0V – 5.5V @ 20 mA
Fabricated using high speed SiGe process

APPLICATIONS

RF transmitter PA setpoint control and level monitoring
RSSI measurement in base stations, WLAN, WiMAX, radar

FUNCTIONAL BLOCK DIAGRAM

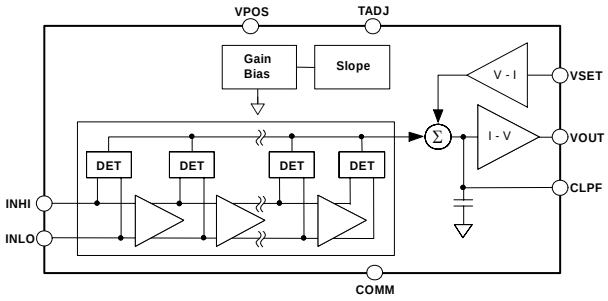

Figure 1. Functional Block Diagram

GENERAL DESCRIPTION

The AD8317 is a demodulating logarithmic amplifier, capable of accurately converting an RF input signal to a corresponding decibel-scaled output. It employs the progressive compression technique over a cascaded amplifier chain, each stage of which is equipped with a detector cell. The device can be used in either measurement or controller modes. The AD8317 maintains accurate log conformance for signals of 1 MHz to 8 GHz and provides useful operation to 10 GHz. The input dynamic range is typically 50 dB (re: 50 Ω) with error less than ±1 dB. The AD8317 has 8-10 ns response time that enables RF burst detection to beyond 125 MHz. The device provides unprecedented logarithmic intercept stability versus ambient temperature conditions. A supply of 3.0V – 5.5 V is required to power the device. Current consumption is typically 20 mA. Power consumption decreases to <1.0 mW when the device is disabled.

The AD8317 can be configured to provide a control voltage to a power amplifier or a measurement output, from pin VOUT. Since the output can be used for controller applications, special attention has been paid to minimize wideband noise. In this mode, the setpoint control voltage is applied to VSET. The feedback loop through an RF amplifier is closed via VOUT; the output of which regulates the amplifier's output to a magnitude corresponding to V_{SET}. The AD8317 provides 0 V to (V_{POS} – 0.4V) output capability at the VOUT pin, suitable for controller applications. As a measurement device, VOUT is externally connected to VSET to produce an output voltage V_{OUT} that is a decreasing linear-in-dB function of the RF input signal amplitude.

The logarithmic slope is –25 mV/dB, determined by the VSET interface. The intercept is +20 dBm (re: 50 Ω, CW input) using the INHI input. These parameters are very stable against supply and temperature variations.

The AD8317 is fabricated on a SiGe bipolar IC process and is available in a 2 × 3 mm, 8-pin LFCSP package, for an operating temperature range of –40°C to +85°C.

Rev. PrE

One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106, U.S.A.
Tel: 781.329.4700 **www.analog.com**
Fax: 781.326.8703

TABLE OF CONTENTS

SPECIFICATIONS

Table 1. V_P = 5 V, C_{LPF} = 220 pF, T_A = 25°C, 52.3 Ω termination resistor at INHI, unless otherwise noted.

Parameter	Conditions	Min	Typ	Max	Unit
SIGNAL INPUT INTERFACE	INHI (Pin 1)				
Specified Frequency Range		0.001		10	GHz
DC Common-Mode Voltage			VPOS – 1.6		V
MEASUREMENT MODE	VOUT (Pin 5) shorted to VSET (Pin 4), Sinusoidal Input Signal				
f = 900 MHz	TADJ = 500 Ω				
Input Impedance			TBD		Ω||pF
± 1 dB Dynamic Range	T_A = +25°C		50		dB
	-40°C < TA < +85°C		TBD		dB
Maximum Input Level	± 1 dB Error		–1		dBm
Minimum Input Level	± 1 dB Error		–51		dBm
Slope		TBD	–23.0	TBD	mV/dB
Intercept		TBD	14	TBD	dBm
Output Voltage - High Power In	P_{IN} = –10dBm	TBD	0.56	TBD	V
Output Voltage - Low Power In	P_{IN} = –40dBm	TBD	1.25	TBD	V
Temperature Sensitivity	P_{IN} = –10dBm				
	25°C ≤ T_A ≤ +85°C		TBD		dB/°C
	–10°C ≤ T_A ≤ +25°C				dB/°C
	–40°C ≤ T_A ≤ +25°C		TBD		dB/°C
f = 1.9 GHz	TADJ = 500 Ω				
Input Impedance			TBD		Ω||pF
± 1 dB Dynamic Range	T_A = +25°C		50		dB
	-40°C < T_A < +85°C		TBD		dB
Maximum Input Level	± 1 dB Error		–2		dBm
Minimum Input Level	± 1 dB Error		–52		dBm
Slope		TBD	–24.4	TBD	mV/dB
Intercept		TBD	20.4	TBD	dBm
Output Voltage - High Power In	P_{IN} = –10dBm	TBD	0.73	TBD	V
Output Voltage - Low Power In	P_{IN} = –35dBm	TBD	1.35	TBD	V
Temperature Sensitivity	P_{IN} = –10 dBm				
	25°C ≤ T_A ≤ +85°C		TBD		dB/°C
	–10°C ≤ T_A ≤ +25°C				dB/°C
	–40°C ≤ T_A ≤ +25°C		TBD		dB/°C
f = 2.2 GHz	TADJ = 500 Ω				
Input Impedance			TBD		Ω||pF
± 1 dB Dynamic Range	T_A = +25°C		50		dB
	-40°C < T_A < +85°C		TBD		dB
Maximum Input Level	± 1 dB Error		–2		dBm
Minimum Input Level	± 1 dB Error		-52		dBm
Slope		TBD	–24.4	TBD	mV/dB
Intercept		TBD	19.6	TBD	dBm
Output Voltage - High Power In	P_{IN} = –10 dBm	TBD	0.73	TBD	V
Output Voltage - Low Power In	P_{IN} = –35dBm	TBD	1.34	TBD	V

Parameter	Conditions	Min	Typ	Max	Unit
Temperature Sensitivity	P_{IN} = −10 dBm				
	25°C ≤ T_A ≤ +85°C		TBD		dB/°C
	−10°C ≤ T_A ≤ +25°C				dB/°C
	−40°C ≤ T_A ≤ +25°C		TBD		dB/°C
f = 3.6 GHz	TADJ = 51 Ω				
Input Impedance			TBD		Ω||pF
± 1 dB Dynamic Range	T_A = +25°C		50		dB
	-40°C < T_A < +85°C		TBD		dB
Maximum Input Level	± 1 dB Error		−2		dBm
Minimum Input Level	± 1 dB Error		−52		dBm
Slope			−24.3		mV/dB
Intercept			19.8		dBm
Output Voltage - High Power In	P_{IN} = −10 dBm		0.717		V
Output Voltage- Low Power In	P_{IN} = −40 dBm		1.46		V
Temperature Sensitivity	P_{IN} = −10 dBm				
	25°C ≤ T_A ≤ +85°C		TBD		dB/°C
	−10°C ≤ T_A ≤ +25°C				dB/°C
	−40°C ≤ T_A ≤ +25°C		TBD		dB/°C
f = 5.8 GHz	TADJ = 1000 Ω				
Input Impedance			TBD		Ω||pF
± 1 dB Dynamic Range	T_A = +25°C		50		dB
	-40°C < T_A < +85°C		TBD		dB
Maximum Input Level	± 1 dB Error		−1		dBm
Minimum Input Level	± 1 dB Error		−51		dBm
Slope			−24.3		mV/dB
Intercept			25		dBm
Output Voltage - High Power In	P_{IN} = −10dBm		0.86		V
Output Voltage- Low Power In	P_{IN} = −40dBm		1.59		V
Temperature Sensitivity	P_{IN} = −10dBm				
	25°C ≤ T_A ≤ +85°C		TBD		dB/°C
	−10°C ≤ T_A ≤ +25°C				dB/°C
	−40°C ≤ T_A ≤ +25°C		TBD		dB/°C
f = 8.0 GHz	TADJ = 500 Ω				
Input Impedance			TBD		Ω||pF
± 1 dB Dynamic Range	T_A = +25°C		TBD		dB
	-40°C < T_A < +85°C		TBD		dB
Maximum Input Level	± 3 dB Error		3		dBm
Minimum Input Level	± 3 dB Error		−47		dBm
Slope			−23		mV/dB
Intercept			37		dBm
Output Voltage - High Power In	P_{IN} = −10dBm		1.06		V
Output Voltage - Low Power In	P_{IN} = −40dBm		1.78		V
Temperature Sensitivity	P_{IN} = −10dBm				
	25°C ≤ T_A ≤ +85°C		TBD		dB/°C
	−10°C ≤ T_A ≤ +25°C				dB/°C
	−40°C ≤ T_A ≤ +25°C		TBD		dB/°C

Parameter	Conditions	Min	Typ	Max	Unit
OUTPUT INTERFACE	VOUT (Pin 5)				
Voltage Swing	VSET = 0 V; RFIN = Open		VPOS – 0.1		V
	VSET = 1.9 V; RFIN = Open		5		mV
Output Current Drive	VSET = 0 V, RFIN = Open		10		mA
Small Signal Bandwidth	RFIN = -10dBm; From CLPF to VOUT		TBD		MHz
Output Noise	RF Input = 2.2 GHz, –10 dBm, f_{NOISE} = 100 kHz, CLPF = TBD		TBD		nV/√Hz
Fall Time	Input Level = No signal to –10 dBm, 90 to 10%; C_{LPF} = 8pF		18		ns
Fall Time	Input Level = No signal to –10 dBm, 90 to 10%; C_{LPF} = open; R_{OUT} = 150 Ohms		6		ns
Rise Time	Input Level = –10 dBm to no signal, 10 to 90%; C_{LPF} = 8pF		20		ns
Rise Time	Input Level = –10 dBm to no signal, 10 to 90%; C_{LPF} = open; R_{OUT} = 150 Ohms		8		ns
VSET INTERFACE	VSET (Pin 4)				
Nominal Input Range	RFIN = 0 dBm; measurement mode		0.4		
	RFIN = –65 dBm; measurement mode		1.4		V
Logarithmic Scale Factor			–0.043		dB/mV
Input Resistance	RFIN = -20dBm; controller mode; VSET = 1V		40		KΩ
TADJ INTERFACE	TADJ (Pin 6)				
Nominal Input Range	Min range		TBD		V
	Max range		TBD		V
Input Resistance	TADJ = 0.9V, Sourcing 50uA		18		KΩ
POWER INTERFACE	VPOS (Pin 7)				
Supply Voltage		3.0		5.5	V
Quiescent Current			22		mA
vs. Temperature	$–40°C \le T_A \le +85°C$		TBD		mA
Disable Current	TADJ = VPOS		200		uA

ABSOLUTE MAXIMUM RATINGS

Table 2. AD8317 Absolute Maximum Ratings

Parameter	Rating
Supply Voltage: VPOS	5.7 V
VSET Voltage	0 to VP
Input Power (Single-ended, re: 50 Ω)	12 dBm
Internal Power Dissipation	0.73
θ_{JA}	55 °C/W
Maximum Junction Temperature	125°C
Operating Temperature Range	–40°C to +85°C
Storage Temperature Range	–65°C to +150°C
Lead Temperature Range (Soldering 60 sec)	260°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although this product features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTIONAL DESCRIPTIONS

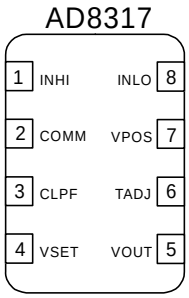

Figure 2. 8-Lead Leadframe Chip Scale Package (LFCSP)

Table 3. Pin Function Descriptions

Pin No.	Mnemonic	Function
7	VPOS	Positive supply voltage: 3.0 V to 5.5 V
3	CLPF	Loop Filter Capacitor
5	VOUT	Measurement and Controller output
4	VSET	Setpoint control input for controller mode, or feedback input for measurement mode
2	COMM	Device common
6	TADJ	Temperature compensation adjustment
1	INHI	RF input. Nominal input range −50 dBm to 0 dBm re: 50 Ω; ac-coupled RF input
8	INLO	RF Common for INHI; ac-coupled RF common
	Paddle	Internally connected to COMM, solder to ground

TYPICAL PERFORMANCE CHARACTERISTICS

V_P = 5 V, T = 25°C, −40°C, +85°C; C_{LPF} = 0.1 uF; T_{ADJ} = 10K Ω; unless otherwise noted. Colors: 25°C → Black; -40°C → Blue; 85°C → Red

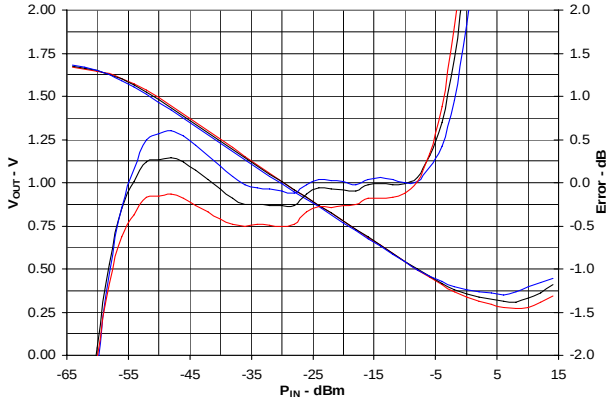

Figure 3: V_{OUT} and Log Conformance vs. Input Amplitude at 900 MHz

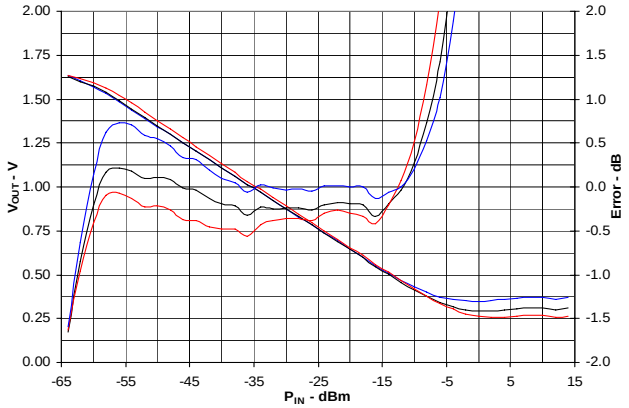

Figure 4: V_{OUT} and Log Conformance vs. Input Amplitude at 3.6 GHz, T_{ADJ} = 18K Ω

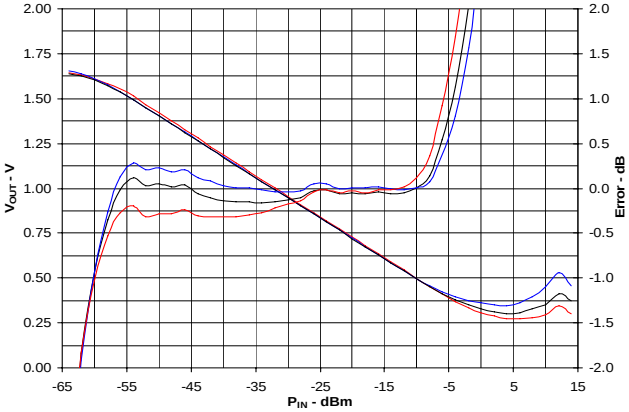

Figure 5: V_{OUT} and Log Conformance vs. Input Amplitude at 1.9 GHz

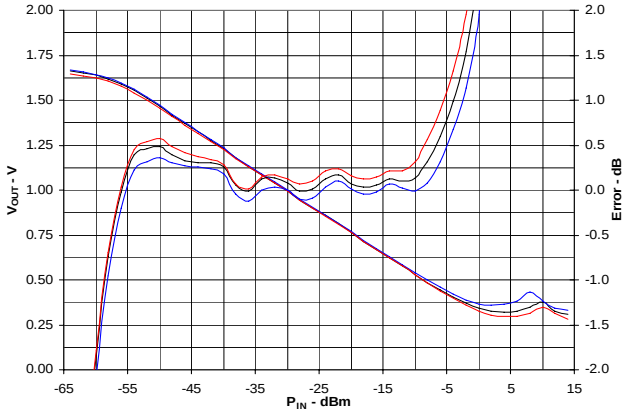

Figure 6: V_{OUT} and Log Conformance vs. Input Amplitude at 5.8 GHz, T_{ADJ} = 1K Ω

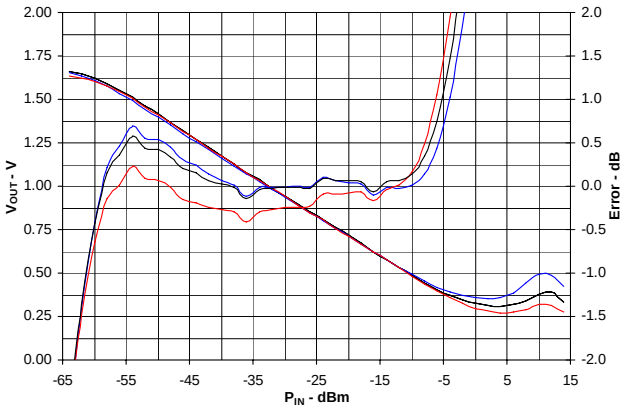

Figure 7: V_{OUT} and Log Conformance vs. Input Amplitude at 2.2 GHz

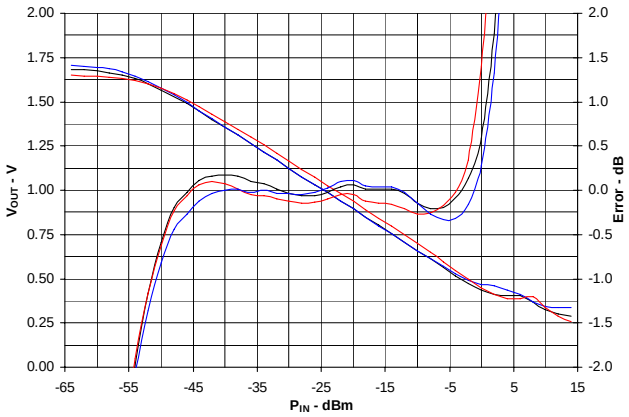

Figure 8: V_{OUT} and Log Conformance vs. Input Amplitude at 8.0 GHz, T_{ADJ} = 28K Ω

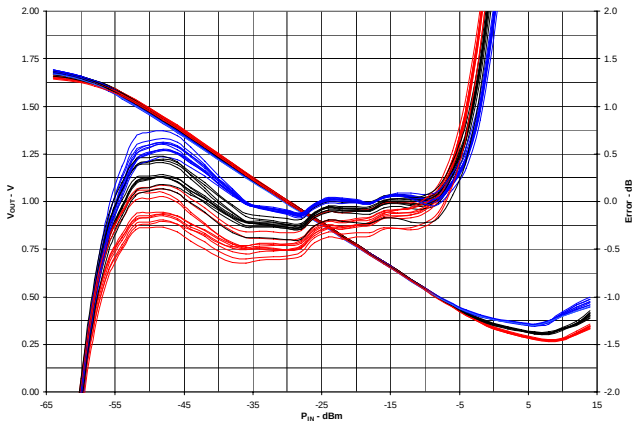

Figure 9: V_{OUT} and Log Conformance vs. Input Amplitude at 900 MHz , Multiple Devices

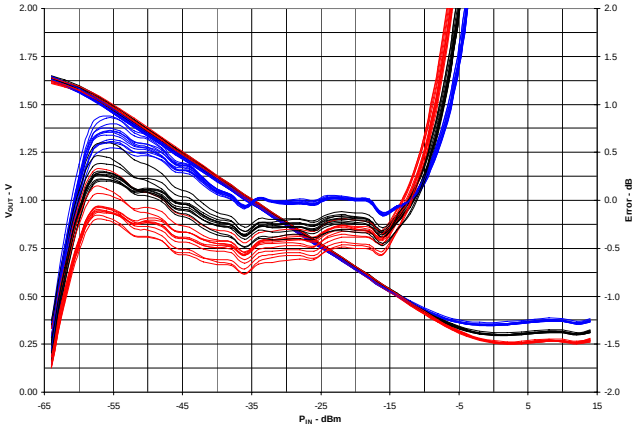

Figure 10: V_{OUT} and Log Conformance vs. Input Amplitude at 3.6 GHz, Multiple Devices, T_{ADJ} = 18K Ω

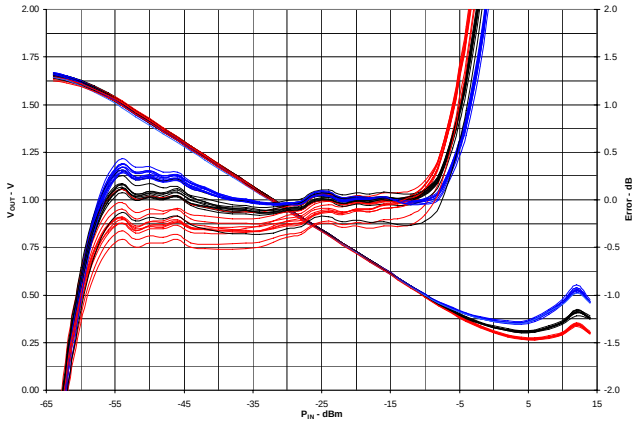

Figure 11: V_{OUT} and Log Conformance vs. Input Amplitude at 1.9 GHz, Multiple Devices

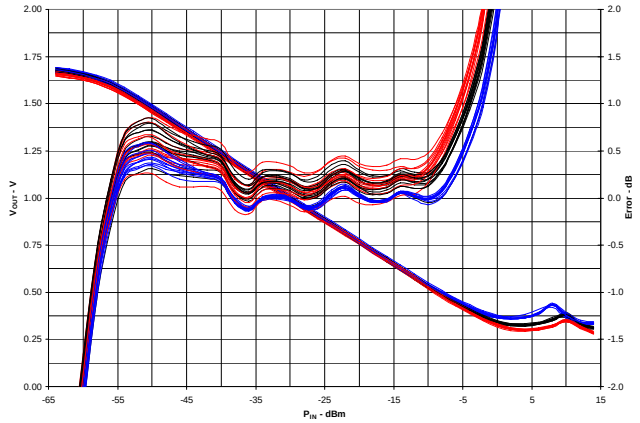

Figure 12: V_{OUT} and Log Conformance vs. Input Amplitude at 5.8 GHz, Multiple Devices , T_{ADJ} = 1K Ω

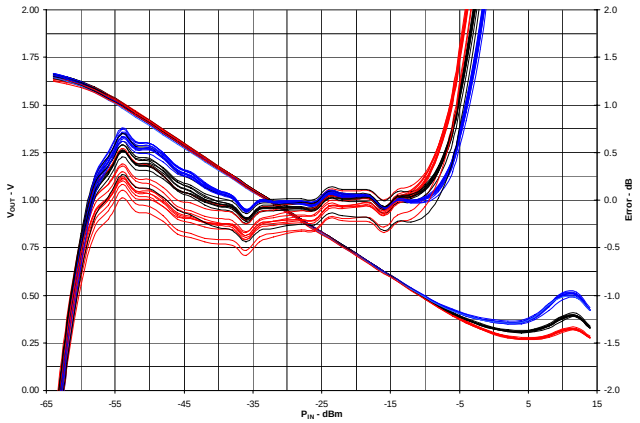

Figure 13: V_{OUT} and Log Conformance vs. Input Amplitude at 2.2 GHz, Multiple Devices

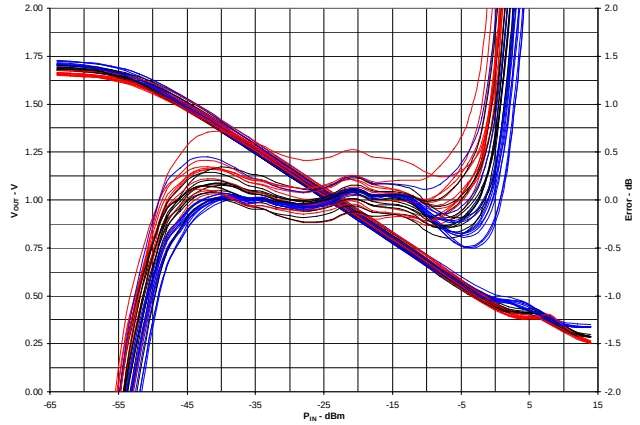

Figure 14: V_{OUT} and Log Conformance vs. Input Amplitude at 8.0 GHz, Multiple Devices, T_{ADJ} = 28K Ω

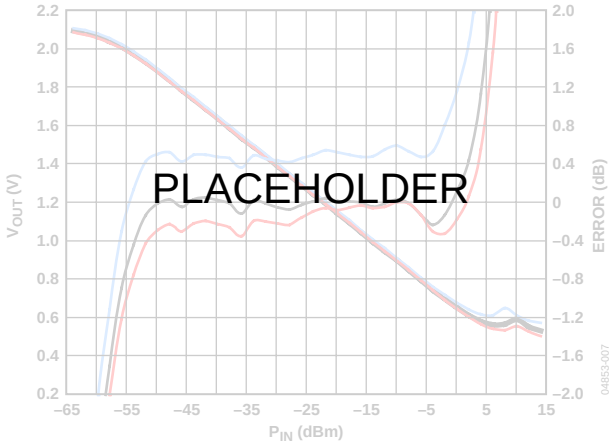

Figure 15: Input Impedance vs. Frequency; No Termination Resistor on INHI

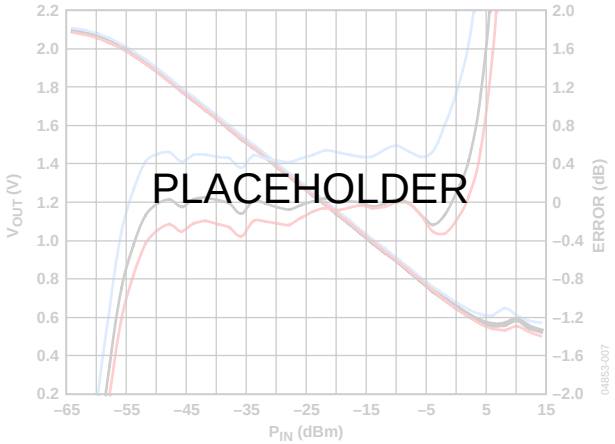

Figure 16: Noise Spectral Density of Output; C_{LPF} = Open

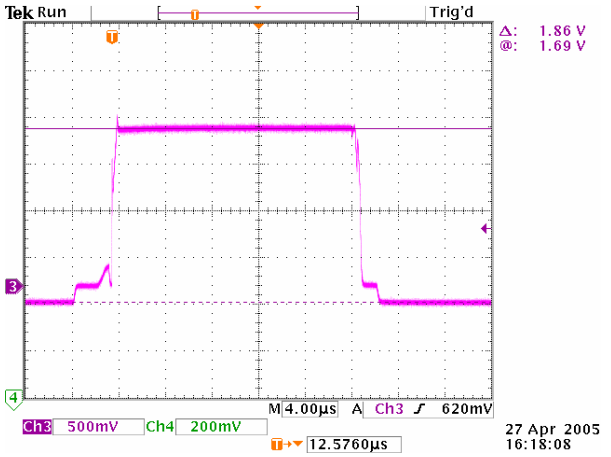

Figure 17: Power On/Off Response Time; V_P = 3.0 V; Input ac-coupling caps = 10pF; C_{LPF} = Open

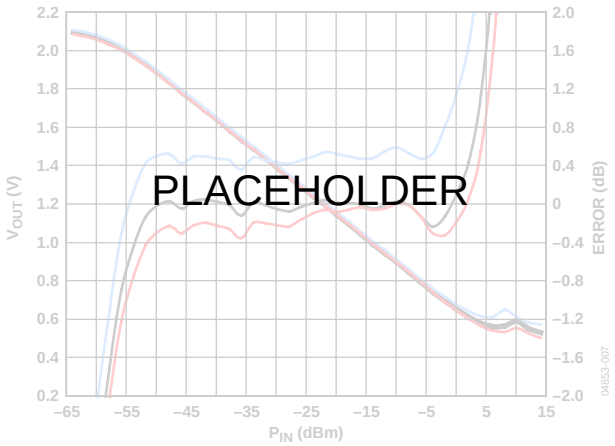

Figure 18: Noise Spectral Density of Output Buffer (from CLPF to VOUT); C_{LPF} = TBD uF

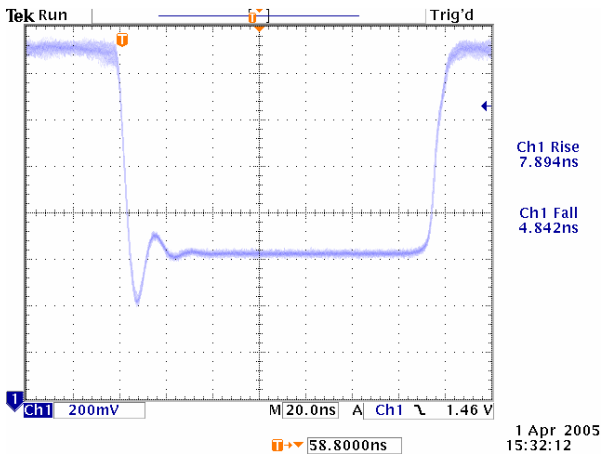

Figure 19: V_{OUT} Pulse Response Time. Pulsed RF Input 0.1 GHz, -10 dBm; C_{LPF} = open; R_{LOAD} = 150 Ω

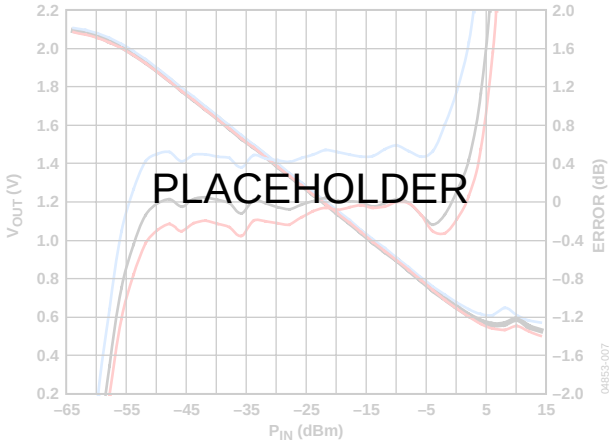

Figure 20: Output Voltage Stability vs. Supply Voltage at 1.9 GHz when V_P varies by 10%, Multiple Devices

GENERAL DESCRIPTION

The AD8317 is a 6-stage demodulating logarithmic amplifier, specifically designed for use in RF measurement and power control applications at frequencies up to 10 GHz. A block diagram is shown in Figure 21. Sharing much of it's design with the AD8318 Logarithmic Detector/Controller, the AD8317 maintains tight intercept variability versus temperature over a 50 dB range. Additional enhancements over the AD8318 such as reduced RF burst response time of 4-6ns, 20mA supply current, and board space requirements of only 2 mm x 3 mm add to the low cost and high performance benefits found in the AD8317.

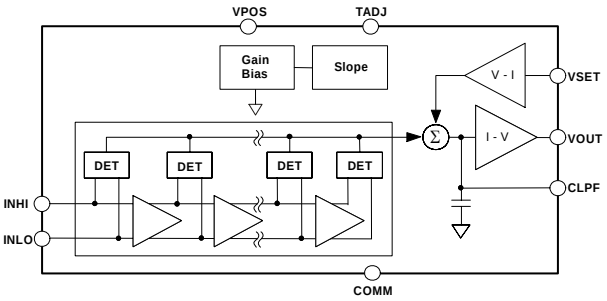

Figure 21: Block Diagram

A fully differential design, using a proprietary high speed SiGe process, extends high frequency performance. Input INHI receives the signal with a low frequency impedance of nominally 500 Ω in parallel with 0.7 pF. The maximum input with +/-1 dB log-conformance error is typically 0 dBm (Re: 50 Ω). The noise spectral density referred to the input is 1.15 nV/√Hz, which is equivalent to a voltage of 118 µV rms in a 10.5 GHz bandwidth, or a noise power of –66 dBm (Re: 50 Ω). This noise spectral density sets the lower limit of the dynamic range. However, the low-end accuracy of the AD8317 is enhanced by specially shaping the demodulating transfer characteristic to partially compensate for errors due to internal noise. The common pin, COMM, provides a quality low impedance connection to the printed circuit board (PCB) ground. The package paddle, which is internally connected to the COMM pin, should also be grounded to the PCB to reduce thermal impedance from the die to the PCB.

The logarithmic function is approximated in a piecewise fashion by 6 cascaded gain stages. (For a more comprehensive explanation of the logarithm approximation, please refer to the AD8307 data sheet, available at www.analog.com.) The cells have a nominal voltage gain of 9 dB each, and a 3 dB bandwidth of 10.5 GHz. Using precision biasing, the gain is stabilized over temperature and supply variations. The overall dc gain is high due to the cascaded nature of the gain stages. An offset compensation loop is included to correct for offsets within the cascaded cells. At the output of each of the gain stages, a square-law detector cell is used to rectify the signal. The RF signal voltages are converted to a fluctuating differential current having an average value that increases with signal level. Along with the six gain stages and detector cells, an additional detector is included at the input of the AD8317, altogether providing a 50 dB dynamic range. After the detector currents are summed and filtered, the function $I_D \times \log_{10}(V_{IN}/V_{INTERCEPT})$ is formed at the summing node, where I_D is the internally set detector current, V_{IN} is the input signal voltage, and $V_{INTERCEPT}$ is the intercept voltage (i.e., when $V_{IN} = V_{INTERCEPT}$, the output voltage would be 0 V, if it were capable of going to 0 V).

USING THE AD8317

BASIC CONNECTIONS

The AD8317 is specified for operation up to 8 GHz, as a result low impedance supply pins with adequate isolation between functions are essential. A power supply voltage of between 3.0 V and 5.5 V should be applied to VPOS. 100 pF and 0.1 µF power supply decoupling capacitors should be connected close to this power supply pin. .

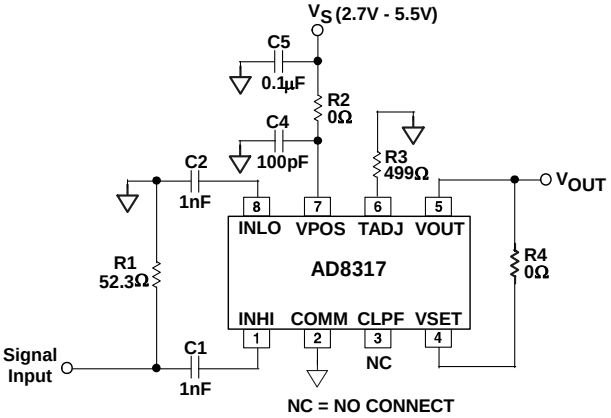

Figure 22: Basic Connections

The paddle of the AD8317's LFCSP package is internally connected to COMM. For optimum thermal and electrical performance, the paddle should be soldered to a low impedance ground plane.

INPUT SIGNAL COUPLING

The RF input to the AD8317 (INHI) is single-ended and must be ac-coupled. INLO (input common) should be ac-coupled to ground. Suggested coupling capacitors are 1 nF ceramic 0402 style capacitors for input frequencies of 1 MHz to 10 GHz. The coupling capacitors should be mounted close to the INHI and INLO pins. The coupling capacitor values can be increased to lower the input stage's high-pass cutoff frequency. The high-pass corner is set by the input coupling capacitors and the internal 10 pF high-pass capacitor. The dc voltage on INHI and INLO will be about one diode voltage drop below V_S.

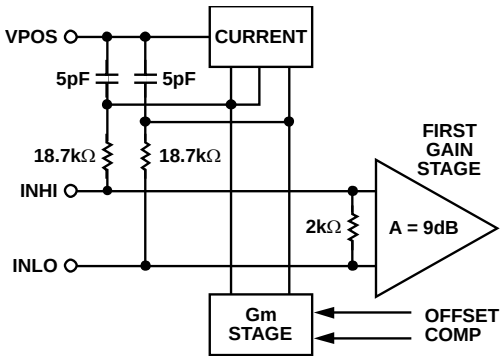

Figure 23: Input Interface

While the input can be reactively matched, in general this is not necessary. An external 52.3 Ω shunt resistor (connected on the signal side of the input coupling capacitors, see Figure 22) combines with the relatively high input impedance to give an adequate broadband 50 Ω match.

OUTPUT INTERFACE

The VOUT pin is driven by a PNP output stage. An internal 10 Ω resistor is placed in series with the emitter follower output and the VOUT pin. The rise time of the output is limited mainly by the slew on CLPF. The fall time is an RC limited slew given by the load capacitance and the pull-down resistance at VOUT. There is an internal pull-down resistor of 1.6 kΩ. Any resistive load at VOUT is placed in parallel with the internal pull-down resistor and provides additional discharge current.

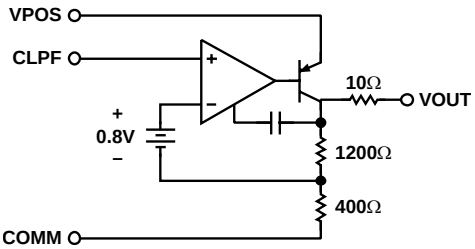

Figure 24: Output Interface

To reduce the fall time, load VOUT with a resistive load of < 1.6 kΩ. For example, with an external load of 200 Ω the AD8317 fall time is < 7nS.

Setpoint Interface

The VSET input drives the high impedance input of an internal op amp. The V_{SET} voltage appears across the internal 1.5 kΩ resistor to generate I_{SET}. When a portion of V_{OUT} is applied to VSET, the feedback loop forces $-I_D \times \log_{10}(V_{IN}/V_{INTERCEPT}) = I_{SET}$. If $V_{SET} = V_{OUT}/2X$, then $I_{SET} = V_{OUT}/(2X \times 1.5\ k\Omega)$.
The result is:

$$V_{OUT} = (-I_D \times 1.5k \times 2X) \times \log_{10}(V_{IN}/V_{INTERCEPT})$$

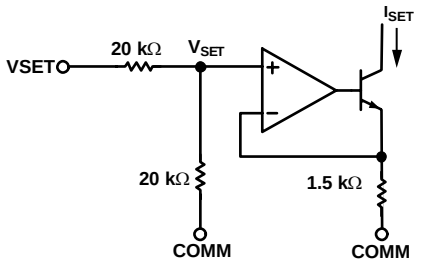

Figure 25: Setpoint Interface

The slope is given by $-I_D \times 2X \times 1.5\ k\Omega = -25mV \times X$. For example, if a resistor divider to ground is used to generate a V_{SET} voltage of $V_{OUT}/2$, then X = 2. The slope will be set to -1V/decade or –50mV/dB.

TEMPERATURE COMPENSATION OF OUTPUT VOLTAGE

The primary component of the variation in V_{OUT} versus temperature, as the input signal amplitude is held constant, is drift of the intercept. This drift is also a weak function of the input signal frequency, so provision is made for optimization of internal temperature compensation at a given frequency by providing pin TADJ.

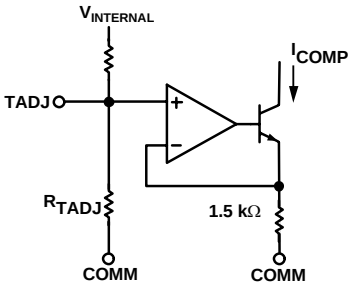

Figure 26: TADJ Interface

The resistor R_{TADJ} is connected between this pin and ground. The value of this resistor partially determines the magnitude of an analog correction coefficient, which is employed to reduce intercept drift.

The relationship between output temperature drift and frequency is not linear and cannot be easily modeled. As a result, experimentation is required to choose the correct T_{ADJ} resistor.

Table 4 shows the recommended values for some commonly used frequencies.

Table 4: Recommended T_{ADJ} Resistor Values

Frequency	Recommended R_{TADJ}
100 MHz	10 kΩ
900 MHz	10 kΩ
1.8 GHZ	10 kΩ
1.9 GHz	10 kΩ
2.2 GHz	10 kΩ
3.6 GHz	18 kΩ
5.3 GHZ	1 kΩ
5.8 GHz	1 kΩ
8 GHz	28 kΩ
10 GHz	TBD Ω

MEASUREMENT MODE

When the V_{OUT} voltage or a portion of the V_{OUT} voltage is fed back to the VSET pin, the device operates in measurement mode. As seen in Figure 27 the AD8317 has an offset voltage, a negative slope, and a V_{OUT} measurement intercept at the high end of its input signal range.

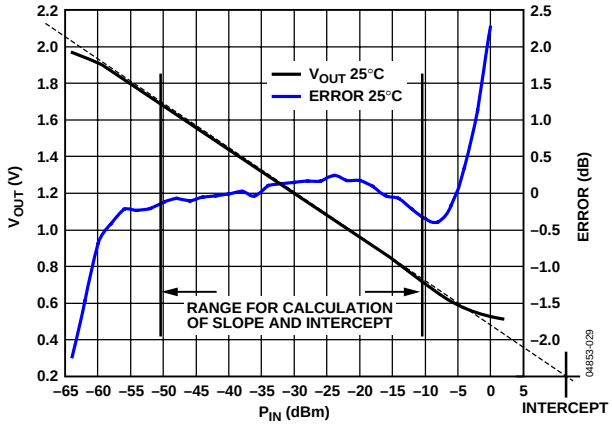

Figure 27: Typical Output Voltage vs. Input Signal

The output voltage versus input signal voltage of the AD8317 is linear-in-dB over a multidecade range. The equation for this function is of the form

$$V_{OUT} = X \times V_{SLOPE/DEC} \times \log10(V_{IN}/V_{INTERCEPT}) \quad (1)$$

$$= X \times V_{SLOPE/dB} \times 20 \times \log10(V_{IN}/V_{INTERCEPT}) \quad (2)$$

where

X is the feedback factor in $V_{SET} = V_{OUT}/X$

$V_{SLOPE/DEC}$ is nominally –500 mV/decade

or -25 mV/dB

$V_{INTERCEPT}$ is the x-axis intercept of the linear-in-dB portion of the V_{OUT} *vs.* V_{IN} curve (Figure 27). $V_{INTERCEPT}$ is +7 dBV for a sinusoidal input signal.

An offset voltage, V_{OFFSET}, of 0.5 V is internally added to the detector signal, so that the minimum value for V_{OUT} is $X \times V_{OFFSET}$, so for X = 1, minimum V_{OUT} is 0.5 V.

The slope is very stable versus process and temperature variation. When base-10 logarithms are used, $V_{SLOPE/DECADE}$ represents the "volts/decade." A decade corresponds to 20 dB, $V_{SLOPE/DECADE}/20 = V_{SLOPE/dB}$ represents the slope in "volts/dB." As noted in the equations above, the V_{OUT} voltage has a *negative* slope. This is also the correct slope polarity to control the gain of many power amplifiers in a negative feedback configuration. Since both the slope and intercept vary slightly with frequency, it is recommended to refer to the specification pages for application specific values for slope and intercept.

Although demodulating log amps respond to input signal voltage, not input signal power, it is customary to discuss the amplitude of high frequency signals in terms of power. In this case, the characteristic impedance of the system, Z_o, must be known to convert voltages to their corresponding power levels. The following equations are used to perform this conversion.

$$P(dBm) = 10 \times \log_{10}(V_{rms}^2/(Z_O \times 1\ mW)) \quad (3)$$

$$P(dBV) = 20 \times \log_{10}(V_{rms}/1\ V_{rms}) \quad (4)$$

$$P(dBm) = P(dBV) - 10 \times \log_{10}(Z_O \times 1\ mW/1V_{rms}^2) \quad . \quad (5)$$

For example, $P_{INTERCEPT}$ for a sinusoidal input signal expressed in terms of dBm (decibels referred to 1 mW), in a 50 Ω system is:

$$P_{INTERCEPT}(dBm) = P_{INTERCEPT}\ (dBV) - 10 \times \log10(Zo \times 1\ mW/1V_{rms}^2) \quad (6)$$

$$= +7\ dBV - 10 \times \log_{10}(50 \times 10^{-3}) = +20\ dBm$$

For a square wave input signal in a 200 Ω system,

$$P_{INTERCEPT} = 4\ dBV - 10 \times \log_{10}(200\ \Omega \times 1\ mW/1V_{rms}^2)] = +11\ dBm$$

Further information on the intercept variation dependence upon waveform can be found in the AD8313 and AD8307 data sheets.

SETTING THE OUTPUT SLOPE IN MEASUREMENT MODE

To operate in measurement mode, VOUT must be connected to VSET. Connecting VOUT directly to VSET yields the nominal logarithmic slope of approximately –25 mV/dB. The output swing corresponding to the specified input range will then be approximately 0.5 V to 2.1 V. The slope and output swing can be increased by placing a resistor divider between VOUT and VSET (i.e., one resistor from VOUT to VSET and one resistor from VSET to common). For example, if two equal resistors are used (e.g., 10 kΩ/10 kΩ), the slope will double to approximately –50 mV/dB. The input impedance of VSET is approximately 500 kΩ. Slope setting resistors should be kept below ~50 kΩ to prevent this input impedance from affecting the resulting slope.

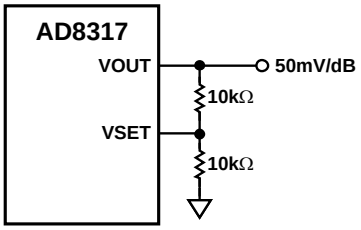

Figure 28: Increasing the Slope

CONTROLLER MODE

The AD8317 provides a controller mode feature at the VOUT pin. Using V_{SET} for the setpoint voltage, it is possible for the AD8317 to control subsystems, such as power amplifiers (PAs), variable gain amplifiers (VGAs), or variable voltage attenuators (VVAs) that have output power that increases monotonically with respect to their gain control signal.

To operate in controller mode, the link between VSET and VOUT is broken. A setpoint voltage is applied to the VSET input; VOUT is connected to the gain control terminal of the variable gain amplifier (VGA) and the detector's RF input is connected to the output of the VGA (usually using a directional coupler and some additional attenuation). Based on the defined relationship between V_{OUT} and the RF input signal when the device is in measurement mode, the AD8317 will adjust the voltage on VOUT (VOUT is now an error amplifier output) until the level at the RF input corresponds to the applied V_{SET}. When the AD8317 operates in controller mode, there is no defined relationship between V_{SET} and V_{OUT} voltage; V_{OUT} will settle to a value that results in the correct input signal level appearing at INHI/INLO.

In order for this output power control loop to be stable, a ground-referenced capacitor must be connected to the C_{FLT} pin.

This capacitor integrates the error signal (which is actually a current) that is present when the loop is not balanced.

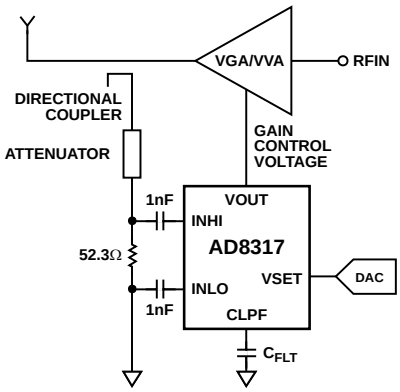

Figure 29: AD8318 Controller Mode

EVALUATION BOARD

Table 5. Evaluation Board (Rev A) Configuration Options

Component	Function	Default Conditions
VPOS, GND	**Supply and Ground Connections**	Not Applicable
R1, C1, C2	**Input Interface:** The 52.3 Ω resistor in position R1 combines with the AD8317's internal input impedance to give a broadband input impedance of around 50 Ω. Capacitors C1 and C2 are DC blocking capacitors. A reactive impedance match can be implemented by replacing R1 with an inductor and C1 and C2 with appropriately-valued capacitors .	R1 = 52.3 Ω (Size 0402) C1 = 1 nF (Size 0402) C2 = 1 nF (Size 0402)
R5, R7	**Temperature Compensation Interface:** The internal temperature compensation network is optimized input signals up to 3.6 GHz when R7 is 10K Ω. This circuit can be adjusted to optimize performance for other input frequencies by changing the value of the resistor in position R7. See Table 4 for specific T_{ADJ} resistor values.	R5 = 200 Ω (Size 0402) R7 = open (Size 0402)
R2, R3, R4, R6, RL, CL	**Output Interface—Measurement Mode:** In measurement mode, a portion of the output voltage is fed back to pin VSET via R2. The magnitude of the slope of the VOUT output voltage response may be increased by reducing the portion of VOUT that is fed back to VSET. R6 can be used as a back-terminating resistor or as part of a single-pole low-pass filter.	R2 = 0 Ω (Size 0402) R3 = open (Size 0402) R4 = open (Size 0402) R6 = 1K Ω (Size 0402 RL = CL = open (Size 0402)
R2, R3	**Output Interface—Controller Mode:** In this mode, R2 must be open. In controller mode, the AD8317 can control the gain of an external component. A setpoint voltage is applied to pin VSET, the value of which corresponds to the desired RF input signal level applied to the AD8317 RF input. A sample of the RF output signal from this variable-gain component is selected, typically via a directional coupler, and applied to AD8317 RF input. The voltage at pin VOUT is applied to the gain control of the variable gain element. A control voltage is applied to pin VSET. The magnitude of the control voltage may optionally be attenuated via the voltage divider comprised of R2 and R3, or a capacitor may be installed in position R3 to form a low-pass filter along with R2.	R2 = open (Size 0402) R3 = open (Size 0402)
C4, C5,	**Power Supply Decoupling:** The nominal supply decoupling consists of a 100 pF filter capacitor placed physically close to the AD8317, and a 0.1 µF capacitor placed nearer to the power supply input pin.	C5 = 100 pF (Size 0402) C4 = 0.1 µF (Size 0603)
C3	**Filter Capacitor:** The low-pass corner frequency of the circuit that drives pin VOUT can be lowered by placing a capacitor between CLPF and ground. Increasing this capacitor will increase the overall rise/fall time of the AD8317 for pulsed input signals.	C3 = 8.2 pF (Size 0402)

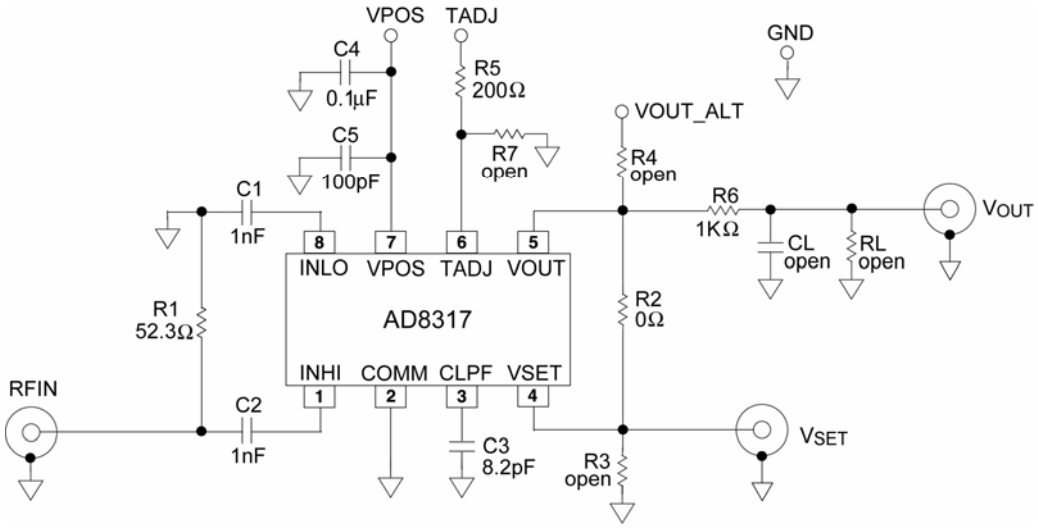

Figure 30. Evaluation Board Schematic (Rev A)

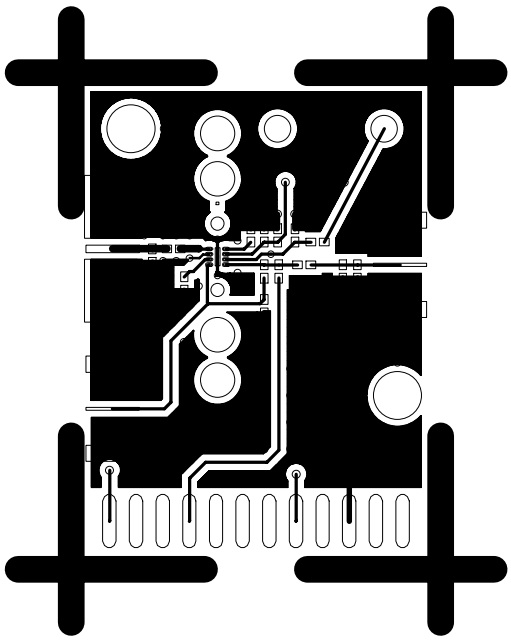

Figure 31: Component Side Layout

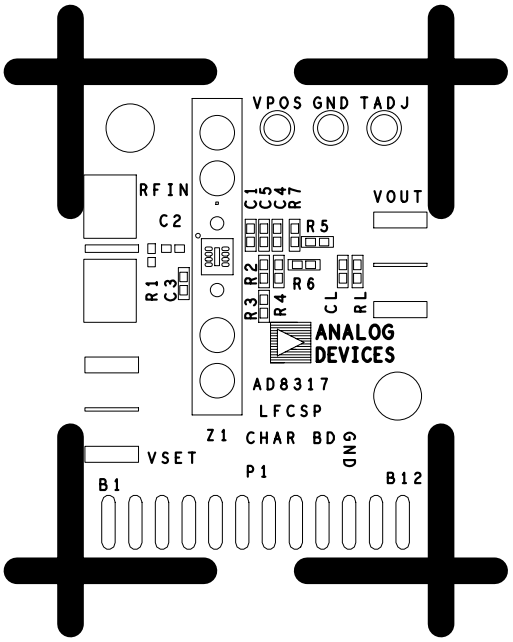

Figure 32: Component Side Silkscreen

OUTLINE DIMENSIONS

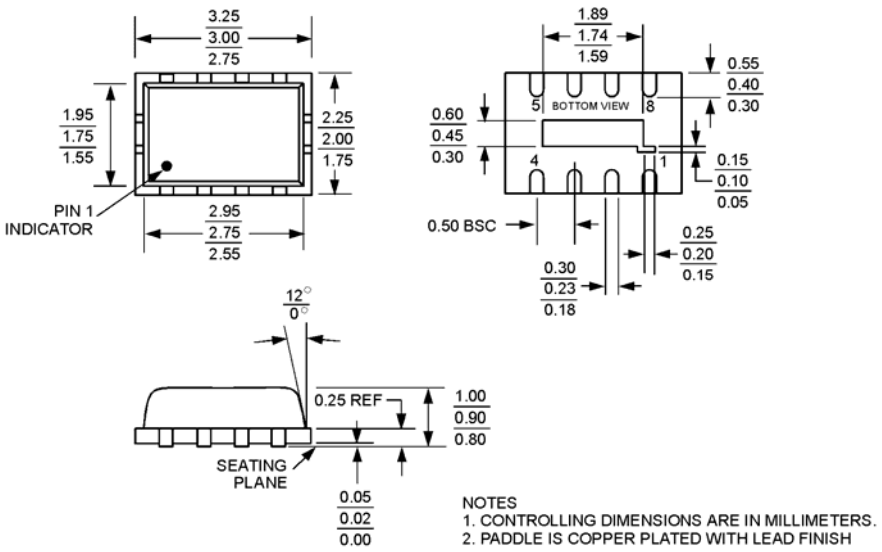

Figure 35. 8-Lead Lead Frame Chip Scale Package

ORDERING GUIDE

AD8317 Products	Temperature Package	Package Description	Package Outline	Branding
AD8317ACPZ[1]-REEL7	–40°C to +85°C	8-Lead LFCSP	CP-8	Q1
AD8317ACPZ[1]-WP	–40°C to +85°C	8-Lead LFCSP	CP-8	Q1
AD8317-EVAL		Evaluation Board		

[1] Z = Pb-free part.

PR05541-0-7/05(PrE)